Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An electronic computer having a program for dividing an application program into a plurality of processing units and generating program data and command code sequences executed by said electronic computer, said computer comprising:

a processing device and a control device;

said processing device including reconfigurable hardware for each of said processing units, wherein said processing device comprises:

a processing element with reconfigurable hardware,

a plurality of program data memories, each holding a program that creates a logic circuit directly in said reconfigurable hardware for each of said processing units,

an effective block selection unit that connects one of said program data memories to said processing element;

said control device executing a command specified by the processing device, wherein said command is instructed to be executed when the processing device detects a predetermined condition and said command includes [[a]] an additional command for execution of switching said programs logically creating the reconfigurable hardware;

said program ~~is given~~ is generated with a control flow of the application program, completion data, structural information of the electronic computer and a plurality of command sets of the electronic computer as inputs; said program executes control flow analysis procedure for dividing the application program into a plurality of said processing units and generating a command sequence intermediate code; and

said program executes a command sequence implementation procedure for translating said command sequence intermediate code into a data string that can be executed by the control device[[;]],

~~said command sequence implementation procedure setting a time period for loading program data of the processing device or making the program data valid; and~~

~~said command sequence implementation procedure executing a program data generation procedure in which the operational content of a processing unit is translated into a data string that can be executed by the processing device.~~

wherein said control device interprets and executes:

an activate command selecting one of said program data memories and activating said processing element to start processing a program held in one of the selected program data memories;

a halt command halting operation of said processing device;

a load_prg command transferring program data from a specified memory device to one of said program data memories, wherein a parameter of the load_prg command indicates a region of one of said program data memories where the program data is stored;

a cancel_prg command canceling a load_prg instruction, and

a wait_prg command waiting until completion of the load_prg instruction.

2-5. (Cancelled).

6. (Previously Presented) The electronic computer as defined in claim 1, comprising a command code memory, holding commands that said control device executes, wherein said control device comprises a command code reference device reading commands from the command code memory according to an address specified by said processing device, interpreting, and executing the commands.

7. (Previously Presented) The electronic computer as defined in claim 6, wherein said command code reference device comprises an address counter holding the address of said command code memory, and in the exchange of commands between said processing device and said control device, a first address control line indicating that an address signal line outputted by said processing device is effective, and a second address counter control line instructing whether the value of the address signal line is stored in the address counter as it is or the result of adding the value of the address signal line to the value of the address counter is stored in the address counter when the first control line is effective.

8. (Previously Presented) The electronic computer as defined in claim 7, wherein said commands are stored in said command code memory in a format comprising a command code that classifies the commands, an address counter control code, and a flag that indicates whether or not the following command is executed, and said address counter control code includes a load_adr command setting the value of the address counter and a add_adr command adding a specified value to the address counter.

9. (Previously Presented) The electronic computer as defined in claim 8, wherein said address counter control code includes a push_adr command that hides the value of the address counter in an address counter stack provided in said control device and that sets a new value to the address counter, and a pop_adr command that returns the value of the address counter stack to the address counter.

10. (Previously Presented) The electronic computer as defined in claim 1, comprising a cache device including a cache memory that temporarily holds data to be transferred to said processing device and a cache controller that controls the cache memory wherein the cache controller is controlled by a command issued by said processing device.

11. (Previously Presented) The electronic computer as defined in claim 10, wherein said cache device comprises an address translation device that translates an address defined externally to said processing device into an address defined inside of the processing device, and the address translation device is controlled by a command issued by said processing device.

12. (Currently Amended) An electronic computer comprising:

a device for dividing an application program into a plurality of processing units;

a processing device including reconfigurable hardware that can create a logic circuit for each said processing unit, having a program, wherein said program is generated, given a control flow of the application program, completion data, structural information of the electronic computer and a plurality of command sets of the electronic computer as inputs, by executing a control flow analysis procedure for generating a command sequence executed after a process,

executing a command sequence implementation procedure for translating said command sequence into a data string, ~~wherein the command sequence implementation procedure sets a time period for loading configuration data of the reconfigurable hardware or making the configuration data valid,~~ and

executing a program data generation procedure for generating program data; and

a control device executing a command specified by the processing device;

wherein said command is instructed to be executed when the processing device detects a predetermined condition and includes a command for execution of switching said programs logically creating the reconfigurable hardware; and

said processing device comprises a second processing device including reconfigurable hardware that can create a logic circuit with a program and a second control device executing a command specified by the second processing device[[.]],

wherein said control device interprets and executes:

an activate command selecting one of said program data memories and activating said processing element to start processing a program held in one of the selected program data memories;

a halt command halting operation of said processing device;

a load_prg command transferring program data from a specified memory device to one of said program data memories, wherein a parameter of the load_prg command indicates a region of one of said program data memories where the program data is stored;

a cancel_prg command canceling a load_prg instruction, and

a wait_prg command waiting until completion of the load_prg instruction.

13. (Previously Presented) A semiconductor integrated circuit implementing the electronic computer as defined in claim 1.

14. (Currently Amended) A control method in an electronic computer for switching and executing programs generated by dividing an application program into a plurality of processing units, wherein said electronic computer includes a control device and a processing device with reconfigurable hardware that can create a logic circuit for each of said processing unit ~~and a control device~~, said method comprising:

issuing an instruction to execute a command when a processing device detects a predetermined condition,

~~and having a program wherein said program is generated~~ generating a program, given a control flow of the application program, completion data, structural information of the electronic computer and a plurality of command sets of the electronic computer as inputs, by executing a control flow analysis procedure for generating a command sequence using ~~executed by~~ said control device,

executing a command sequence implementation procedure for translating said command sequence into a data string, ~~wherein the command sequence implementation procedure sets a time period for loading configuration data of the processing device or making the program data valid, and~~

executing a program data generation procedure for generating program data; [[and]]

executing switching said programs that logically create reconfigurable hardware by said control device that has received the command execution instruction from the processing device[[.]];

interpreting and executing:

an activate command selecting one of said program data memories and activating said processing element to start processing a program held in one of the selected program data memories;

a halt command halting operation of said processing device;

a load_prg command transferring program data from a specified memory device to one of said program data memories, wherein a parameter of the load_prg command indicates a region of one of said program data memories where the program data is stored;

a cancel_prg command canceling a load_prg instruction, and

a wait_prg command waiting until completion of the load_prg instruction.

15. (Previously Presented) The control method as defined in claim 14, wherein, after said switching, while a program in a predetermined program data memory is being executed, a next program is read into another program data memory.

16. (Currently Amended) A control method, in an electronic computer for switching and executing programs generated by dividing an application program into a

plurality of processing units, wherein said electronic computer includes a control device and a processing device with reconfigurable hardware that can create a logic circuit for each of said processing unit ~~and a control device~~, said method comprising:

issuing an instruction to execute a command when a processing device detects a predetermined condition, said processing device including reconfigurable hardware, a plurality of program data memories that hold programs for each said processing unit, wherein said programs are generated, given a control flow of the application program, completion data, structural information of the electronic computer and a plurality of command sets of the electronic computer as inputs, by executing a control flow analysis procedure for generating a command sequence using ~~executed by~~ said control device,

executing a command sequence implementation procedure for translating said command sequence into a data string, [[,]] ~~wherein the command sequence implementation procedure sets a time period for loading configuration data of the reconfigurable hardware or making the configuration data valid,~~ and

executing a program data generation procedure for generating program data,

creating logic circuits of the reconfigurable hardware, and an effective block selection unit that selects one program data memory from the plurality of program data memories and that makes it effective;

executing, by said control device that has received the command execution instruction from the processing device, an activate command controlling the effective block selection unit so as to make a specified program data memory effective and connecting it to the reconfigurable hardware; [[and]]

switching the content of a logic circuit executed by the reconfigurable hardware[[.]];

interpreting and executing:

an activate command selecting one of said program data memories and activating said processing element to start processing a program held in one of the selected program data memories;

a halt command halting operation of said processing device;

a load_prg command transferring program data from a specified memory device to one of said program data memories, wherein a parameter of the load_prg command indicates a region of one of said program data memories where the program data is stored;

a cancel_prg command canceling a load_prg instruction, and

a wait_prg command waiting until completion of the load_prg instruction.

17. (Previously Presented) The control method as defined in claim 16, wherein said control device executes:

a halt command halting the operation of said specified processing device;

an interrupt command issuing an interrupt vector from said control device to said specified processing device;

a load_prg command transferring program data from a specified memory device to said program data memory;

a cancel_prg command canceling a load_prg instruction, and

a wait_prg command waiting until a completion of the load_prg instruction.

18. (Currently Amended) A program generation method for an electronic computer executing an application program divided into a plurality of processing units, wherein said electronic computer includes a processing device with reconfigurable hardware that can create a logic circuit for each of said processing units and a control device, comprising:

analyzing a control;

implementing a command sequence procedure in which a command sequence is generated by translating [[the]] a command sequence intermediate code into a form that can be executed by the electronic computer~~, wherein the command sequence procedure sets a time period for loading configuration data of the reconfigurable hardware or making the configuration data valid~~; and

generating program data in which operational content of a processing unit is translated into a form that can be executed by the electronic computer,

wherein the application program is divided so that each processing unit can be stored in a program data memory that holds a program creating a logic circuit for each processing unit in said reconfigurable hardware when [[the]] a control flow of the application program is analyzed and divided into processing units in said analyzing a control flow ~~analysis procedure~~ step[[.]];

interpreting and executing:

an activate command selecting one of said program data memories and activating said processing element to start processing a program held in one of the selected program data memories;

a halt command halting operation of said processing device;

a load_prg command transferring program data from a specified memory device to one of said program data memories, wherein a parameter of the load_prg command indicates a region of one of said program data memories where the program data is stored;

a cancel_prg command canceling a load_prg instruction, and

a wait_prg command waiting until completion of the load_prg instruction.

19. (Cancelled).

20. (Currently Amended) A computer program product for an electronic computer for switching and executing programs generated by dividing an application program into a plurality of processing units, wherein said electronic computer includes a control device and a processing device with reconfigurable hardware that can create a logic circuit for each of said processing units ~~and a control device~~, embodied in a computer readable medium, which when executed, causes a computer to perform the steps of:

issuing an instruction to execute a command when the processing device detects a predetermined condition,

~~and having a program, wherein said program is generated~~ generating a program, given a control flow of the application program, completion data, structural information of the electronic computer and a plurality of command sets of the electronic computer as inputs, by executing a control flow analysis procedure for generating a command sequence using ~~executed by~~ said control device,

executing a command sequence implementation procedure for translating said command sequence into a data string, ~~wherein the command sequence implementation procedure sets a time period for loading configuration data of the reconfigurable hardware or making the configuration data valid,~~ and

executing a program data generation procedure for generating program data executed by the processing device; [[and]]

executing switching said program that logically creates reconfigurable hardware by said control device that has received the command execution instruction from the processing device[[.]];

interpreting and executing:

an activate command selecting one of said program data memories and activating said processing element to start processing a program held in one of the selected program data memories;

a halt command halting operation of said processing device;

a load_prg command transferring program data from a specified memory device to one of said program data memories, wherein a parameter of the load_prg command indicates a region of one of said program data memories where the program data is stored;

a cancel_prg command canceling a load_prg instruction, and

a wait_prg command waiting until completion of the load_prg instruction.

21. (Currently Amended) A computer program product, for an electronic computer for switching and executing programs generated by dividing an application program into a plurality of processing units, wherein said electronic computer includes a control device and a processing device with reconfigurable hardware that can create a logic circuit for each of said processing units ~~and a control device~~, embodied in a computer readable medium, which when executed causes a computer to perform the steps of:

issuing an instruction to execute a command when the processing device detects a predetermined condition, a plurality of program data memories that hold programs for each said processing unit, wherein said programs are generated, given a control flow of the application program, completion data, structural information of an electronic computer and a plurality of command sets of the electronic computer as inputs, by executing a control flow analysis procedure for generating a command sequence executed after a process,

executing a command sequence implementation procedure for translating said command sequence into a data string, ~~wherein the command sequence implementation procedure sets a time period for loading configuration data of the reconfigurable hardware or making the configuration data valid,~~ and

executing a program data generation procedure for generating program data ~~executed by~~ using the processing device,

creating logic circuits of the reconfigurable hardware, and an effective block selection unit that selects one program data memory from the plurality of program data memories and that makes it effective;

executing, by the control device that has received the command execution instruction from the processing device, an activate command controlling the effective block selection unit so as to make a specified program data memory effective and connecting it to the reconfigurable hardware; [[and]]

switching the content of a logic circuit executed by the reconfigurable hardware[[.]];

interpreting and executing:

an activate command selecting one of said program data memories and activating said processing element to start processing a program held in one of the selected program data memories;

a halt command halting operation of said processing device;

a load_prg command transferring program data from a specified memory device to one of said program data memories, wherein a parameter of the load_prg command indicates a region of one of said program data memories where the program data is stored;

a cancel_prg command canceling a load_prg instruction, and

a wait_prg command waiting until completion of the load_prg instruction.

22. (Currently Amended) The computer program product , embodied in a computer readable medium as defined in claim 21, further comprising computer code which includes a halt command halting operation of said specified processing device, an interrupt command issuing an interrupt vector from said control device to said specified processing device, a load_prg command transferring program data from a specified memory device to said program data memory, a cancel_prg command canceling a load_prg instruction, and a wait_prg command waiting until [[the]] a completion of the load_prg instruction are executed.